IN THE SPECIFICATION

Below are amended paragraphs on pages 3, 15 and 16 of the specification:

Please amend the first full paragraph on page 3 to read:

A large static jitter buffer can be designed into the receiving gateway to optimize performance against large amounts of network delay jitter at the cost of large delays which will be noticed by users; on the other hand, a small jitter buffer can be used which will introduce minimal delays but at the cost of significant packet loss. In this case, ~~and~~ call quality degrades when the network jitter exceeds the size of the jitter buffer.

a1

Please amend the last paragraph on page 15 and the first paragraph on page 16 to read as follows:

FIG. 5a-5c illustrate an exemplary case in which the manager increases jitterbuffer size to compensate for network degradation. FIG. 5a represents the initial situation before network degrades. Jitter buffer 56 includes, initially, eight allocated slots 220 through 227. (In this and the following figures, solidly outlined slots indicate memory which has the incoming packet loaded-filled slots-while phantom outlined slots are "empty" – allocated but still awaiting receipt of corresponding packet data.) Packet 122 loads into a respective buffer slot 222, with offset of two packet periods from the shift output (serial out). Packet arrival variance is two periods. The speed control~~/decoder~~ 62 and decoder 64 reads at the same rate as (average) packet arrival, yielding steady audio with a two packet period delay.

a2

In FIG. 5b, network conditions have decayed somewhat: average delay is now 4 packets, and the variance of the offset is >2. Jitter buffer slots have shifted one period (to the right in the figure) and thus are now numbered 221-230 in recognition that one period had passed since FIG. 5a. Packet 124 is shown arriving late, whereas 126 arrives on center. Both are loaded into corresponding slots in the jitter buffer 56. To compensate for the increased variance, the jitter buffer manager 54 decides to shift the buffer load position to a different slot and increases the size of the buffer by allocating 2 more slots. The manager 54 also sends a control signal to speed control~~/decoder~~ 62 and decoder 64 causing it to slow its rate of